

100

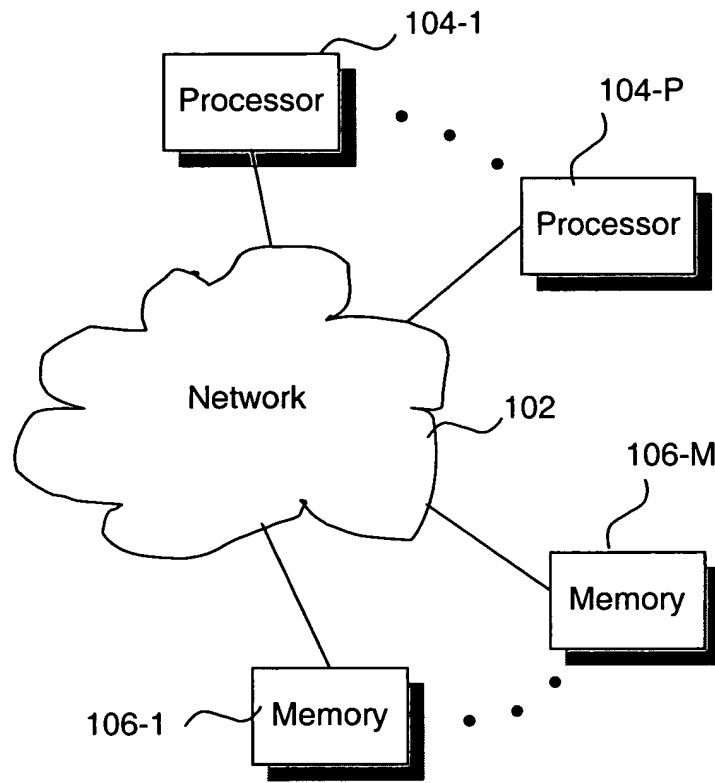


FIG. 1

200

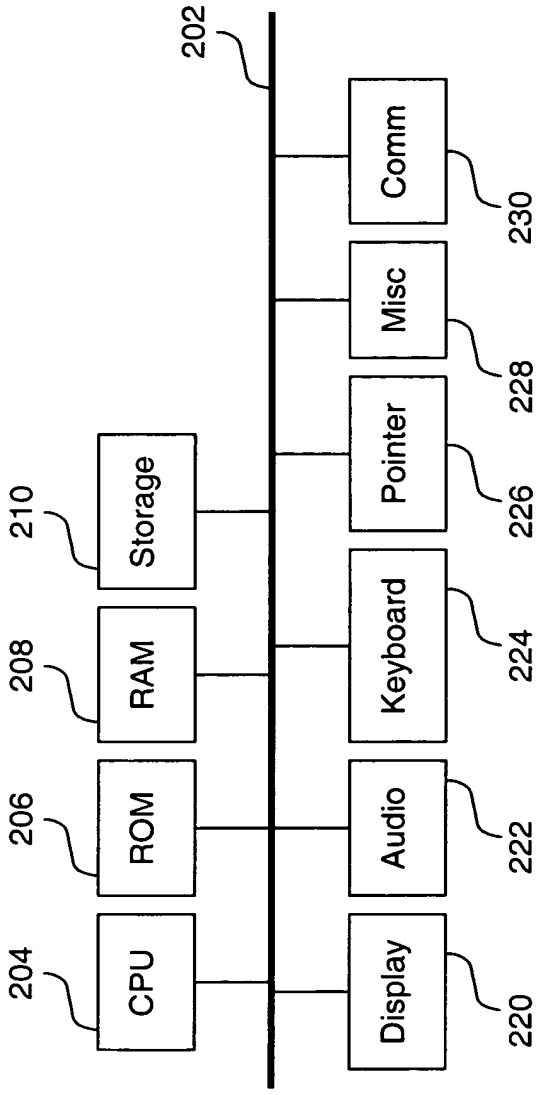


FIG. 2

3/19

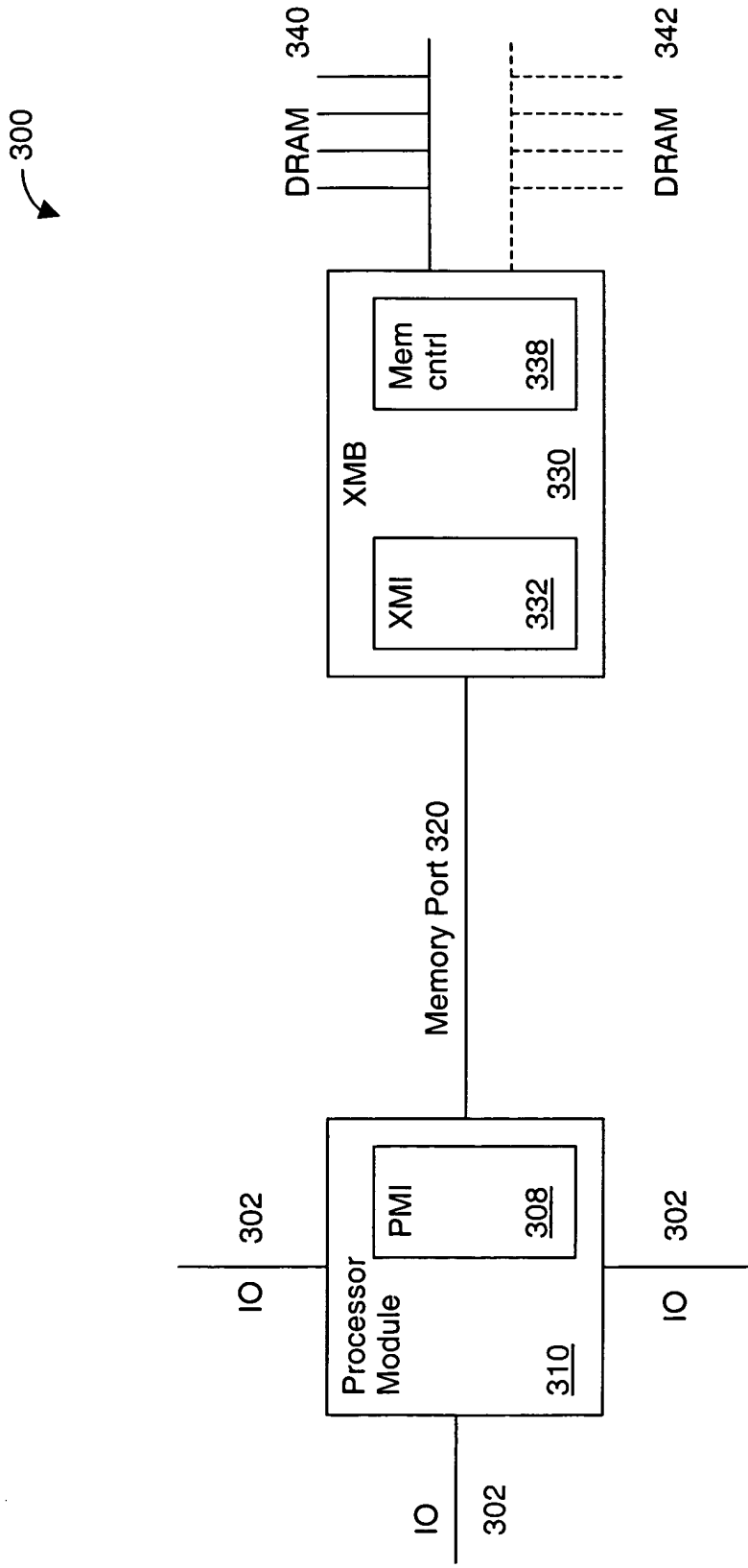


FIG. 3

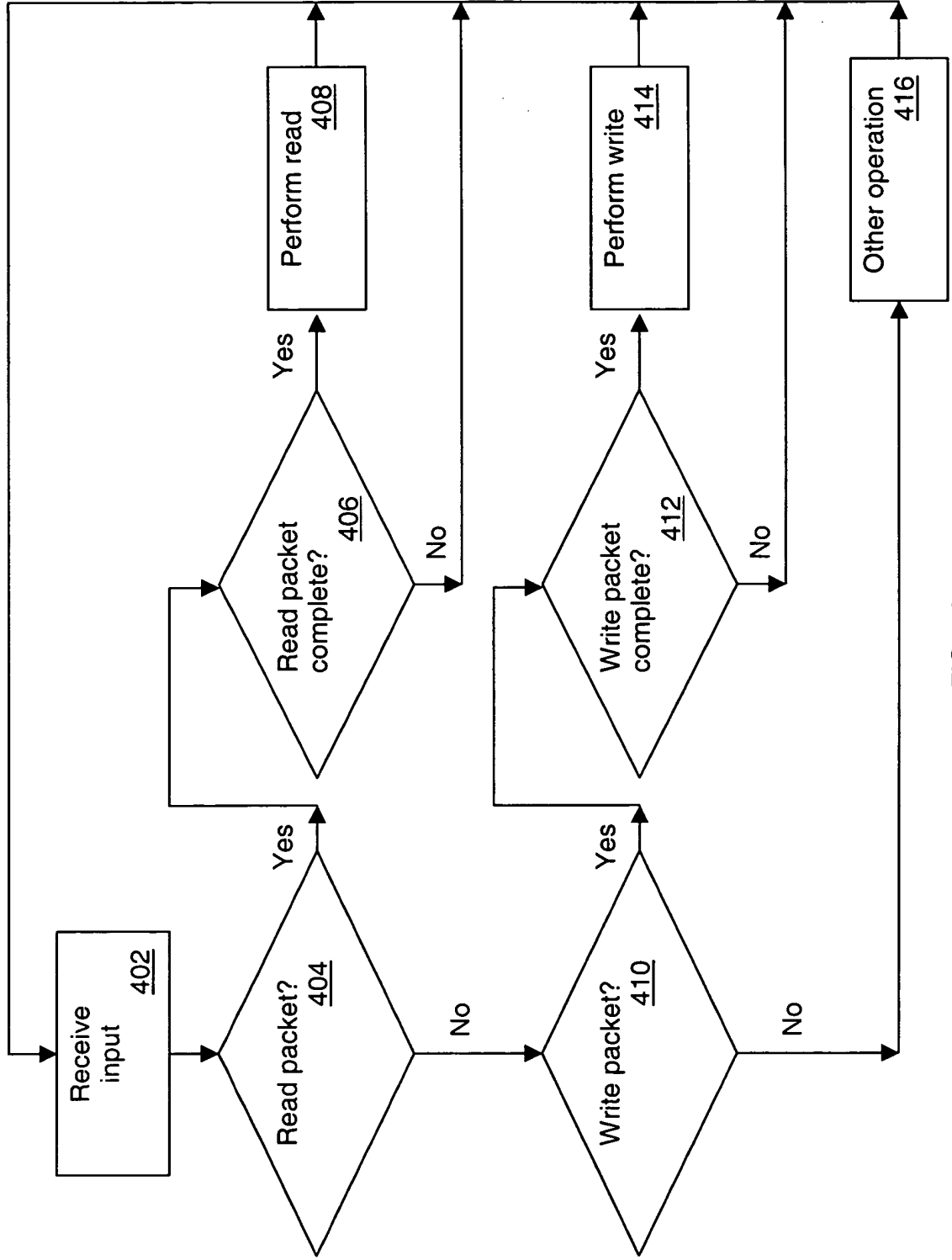


FIG. 4A

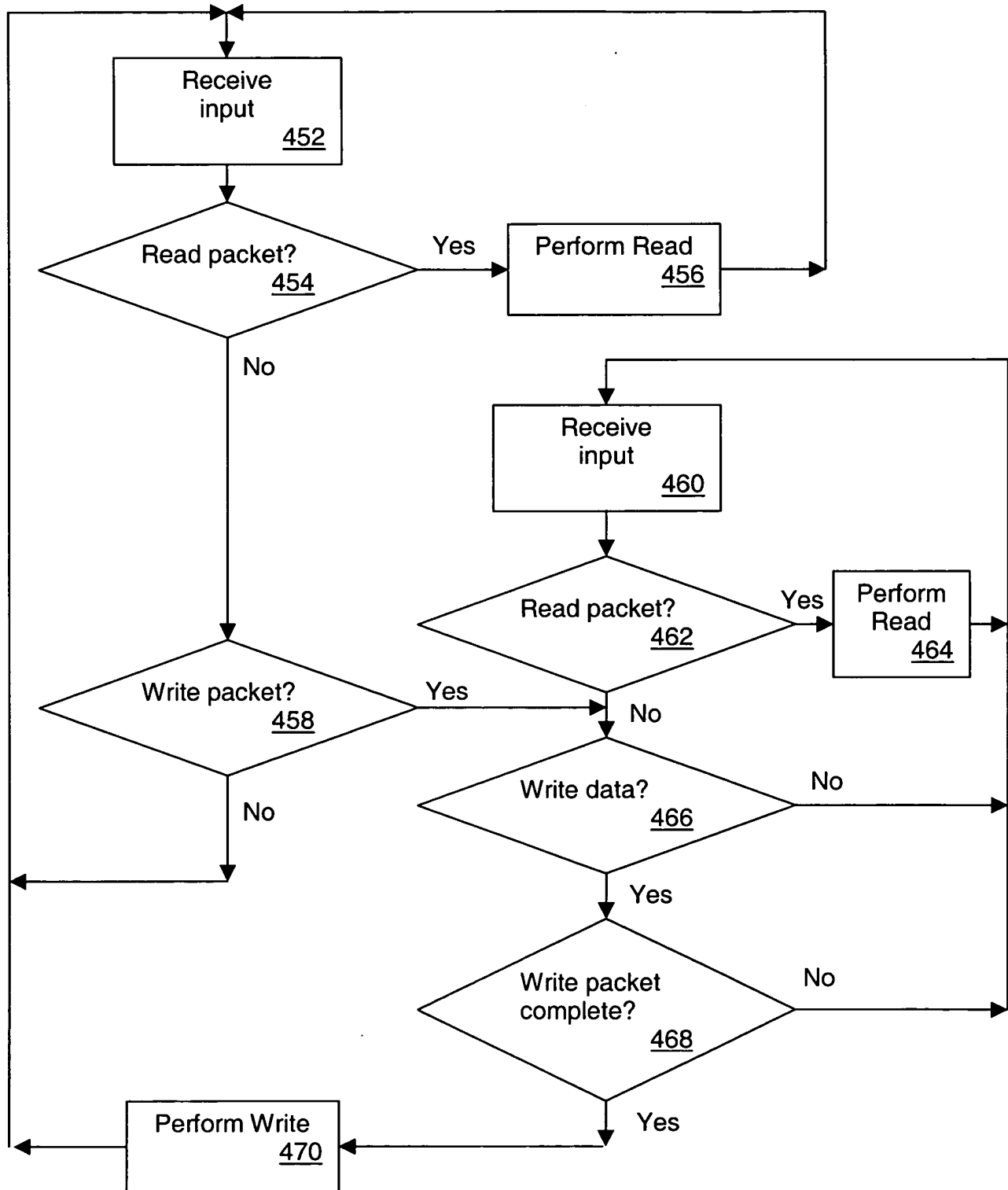


FIG. 4B

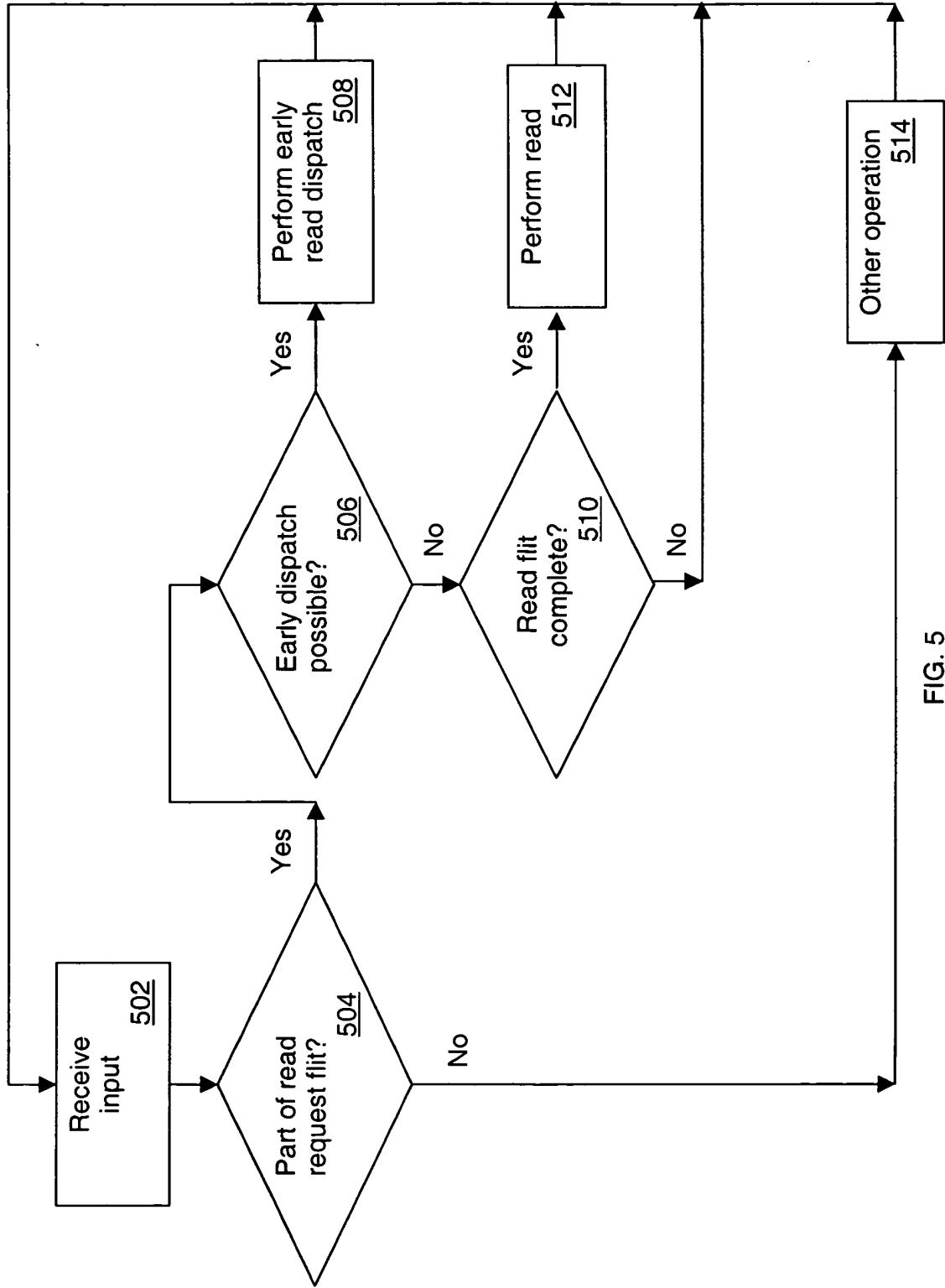


FIG. 5

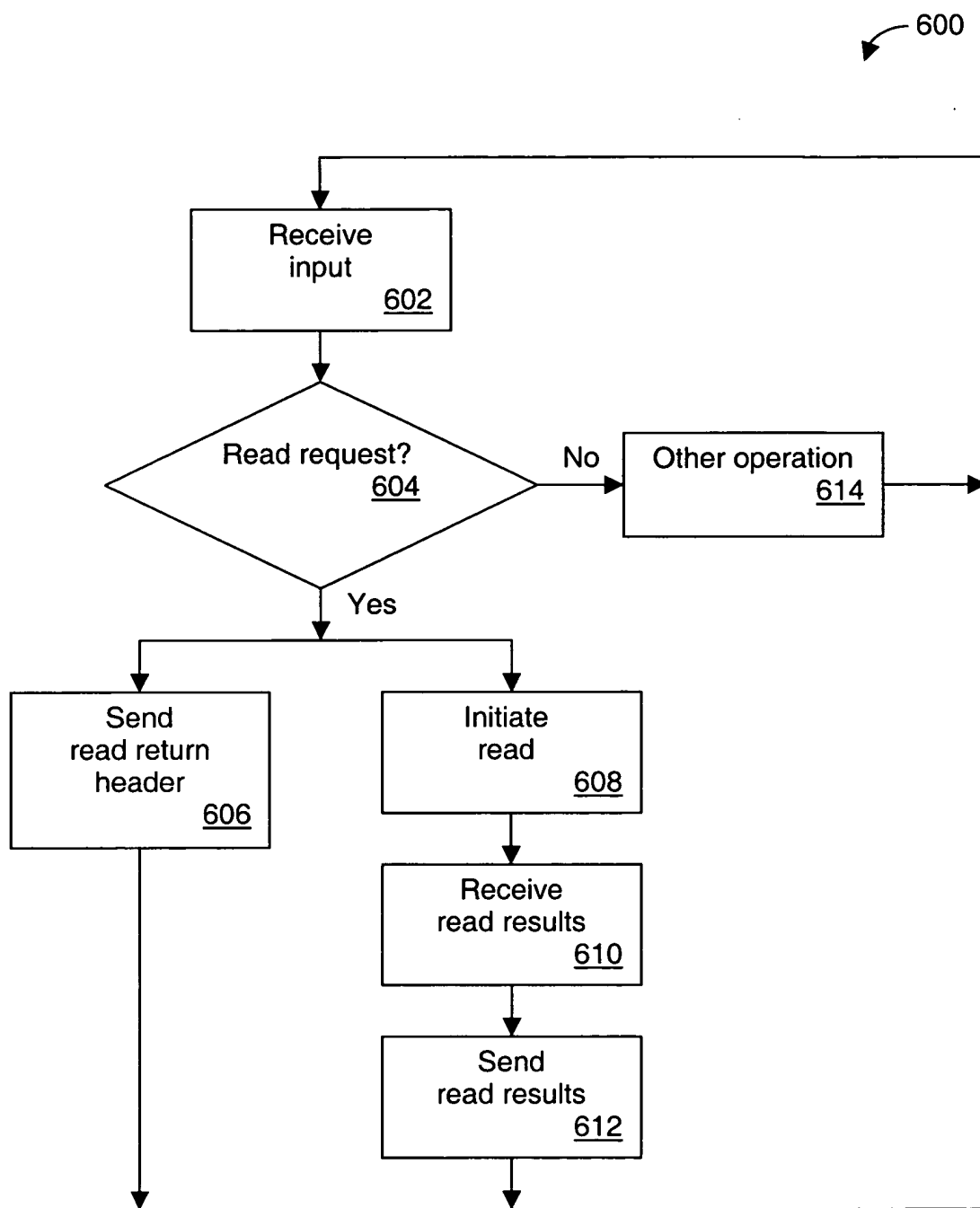


FIG. 6A

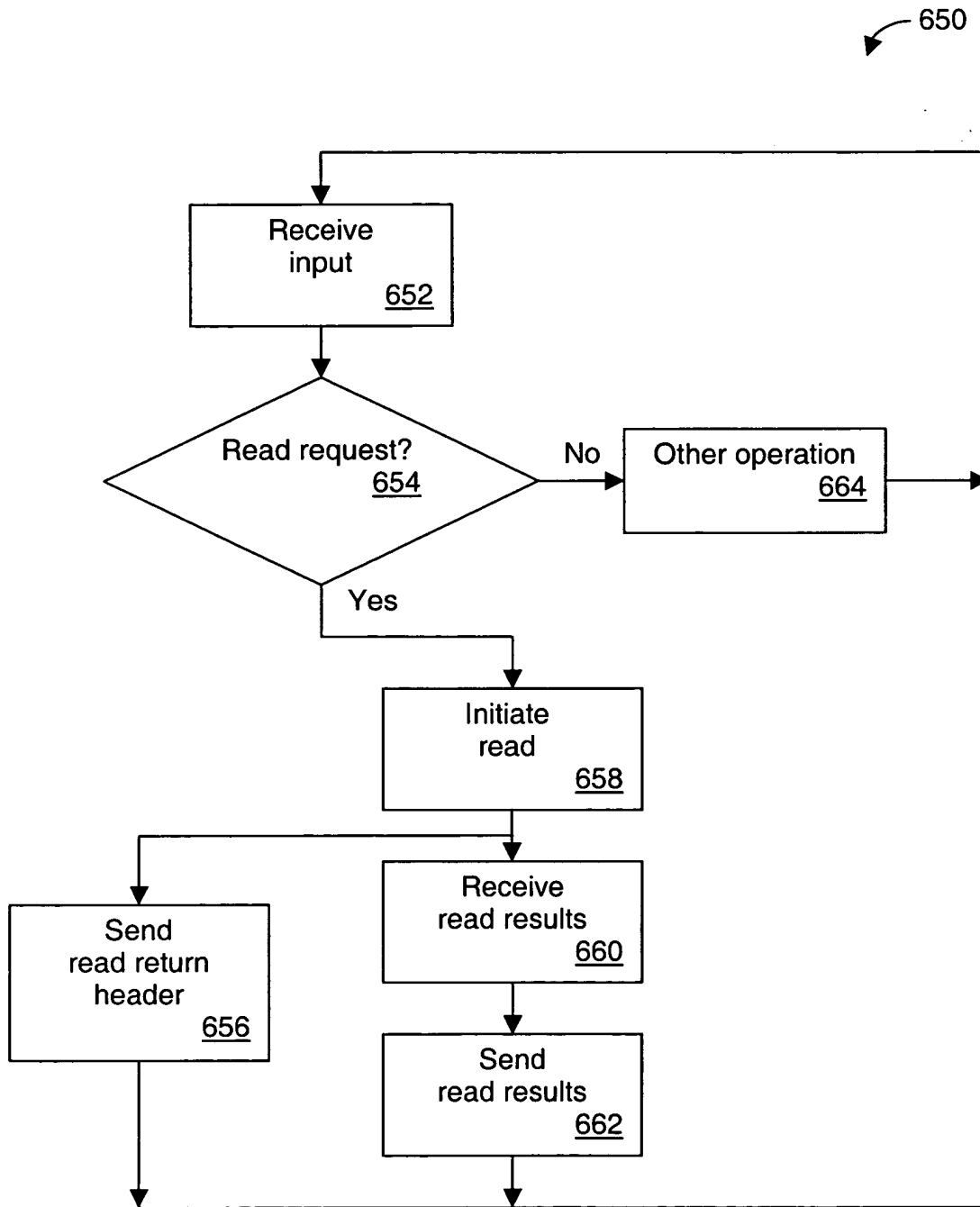


FIG. 6B

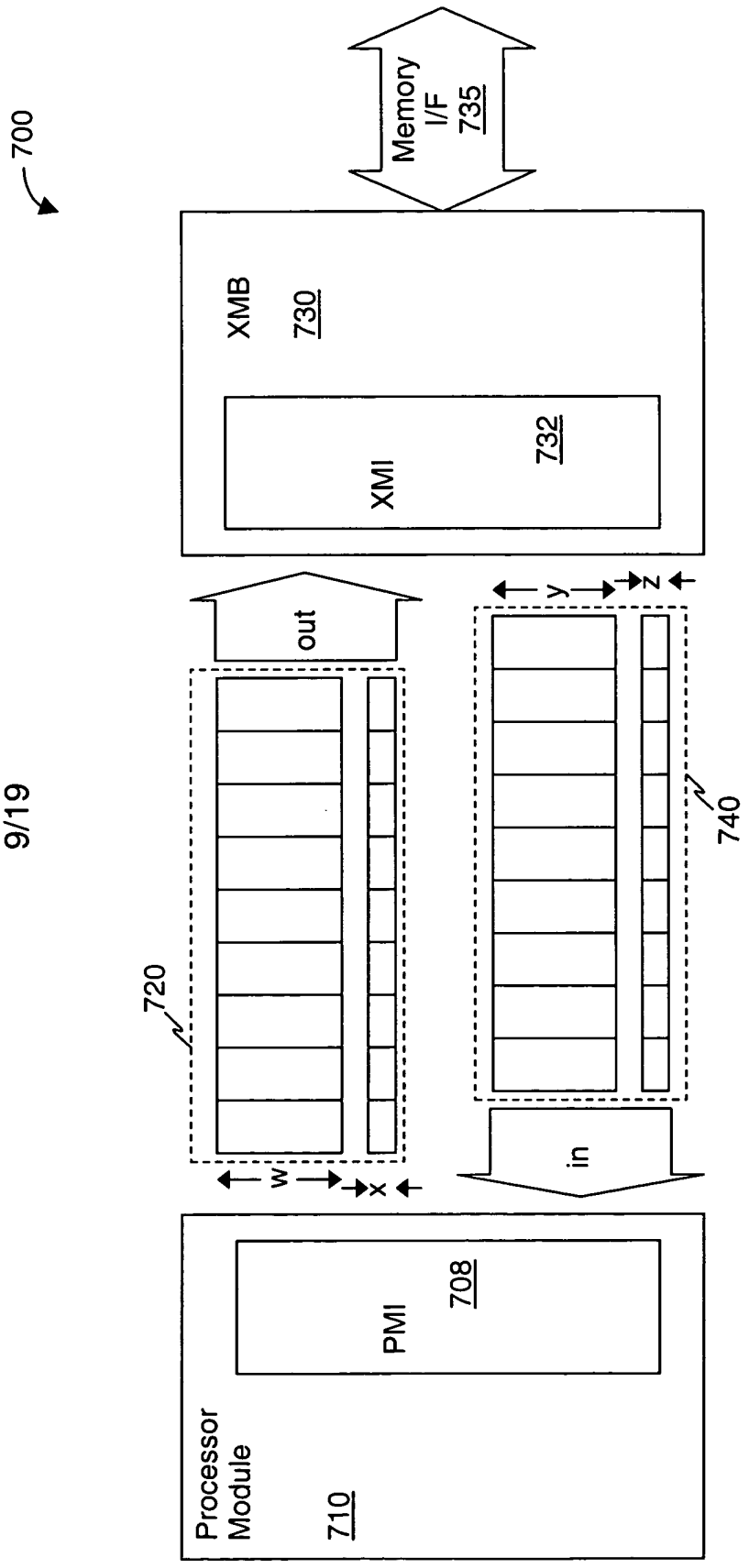


FIG. 7

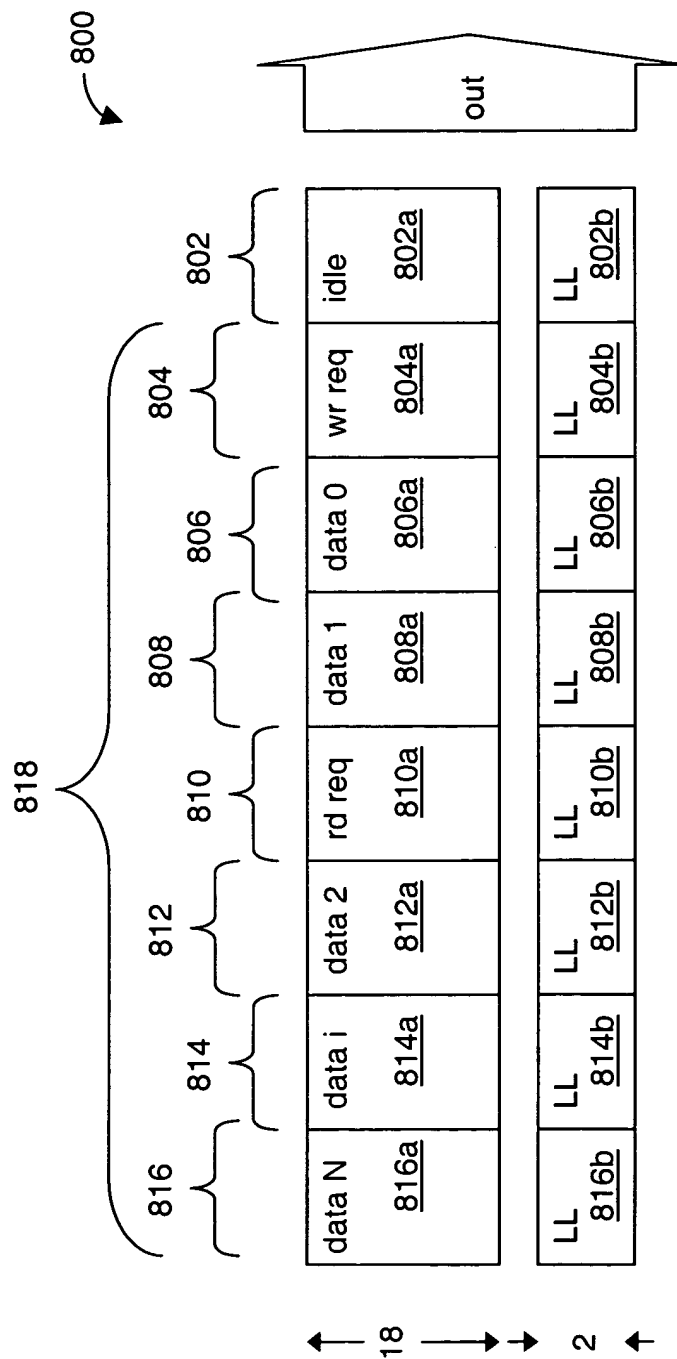


FIG. 8

900

910

18

d/c transfer 3 <u>910a-3</u>	d/c transfer 2 <u>910a-2</u>	d/c transfer 1 <u>910a-1</u>	d/c transfer 0 <u>910a-0</u>
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2

LL transfer 3 <u>910b-3</u>	LL transfer 2 <u>910b-2</u>	LL transfer 1 <u>910b-1</u>	LL transfer 0 <u>910b-0</u>
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FIG. 9

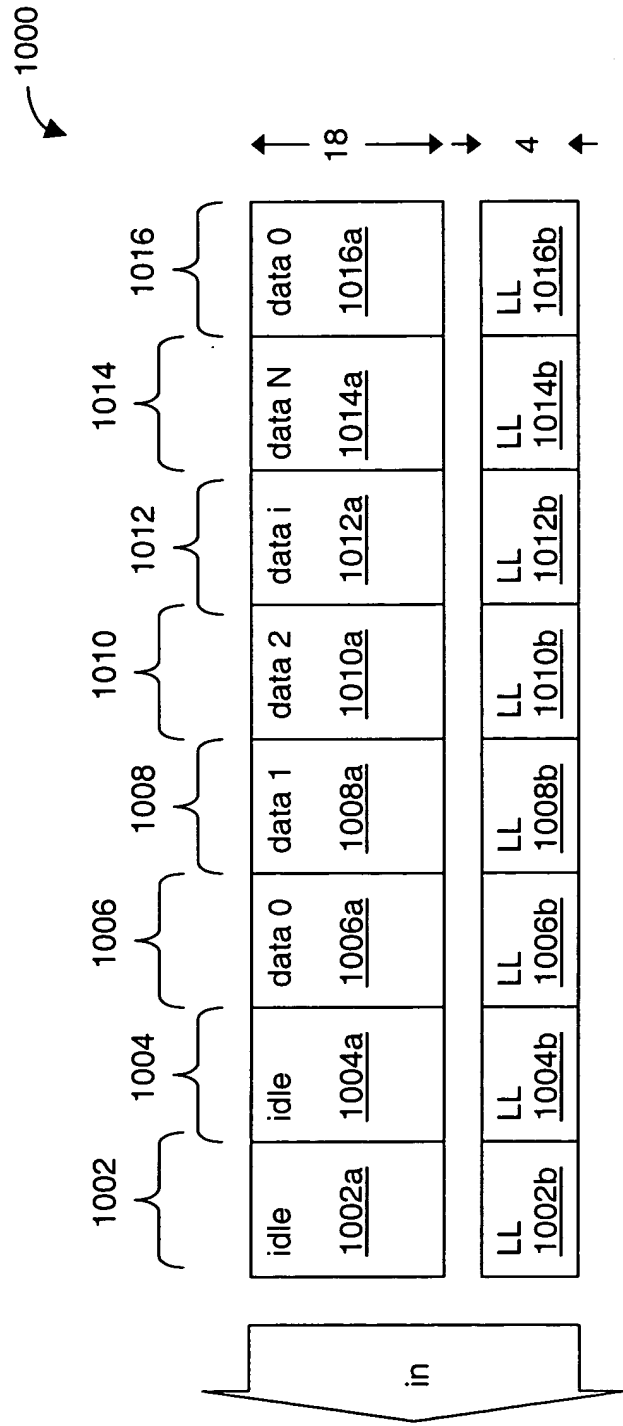


FIG. 10

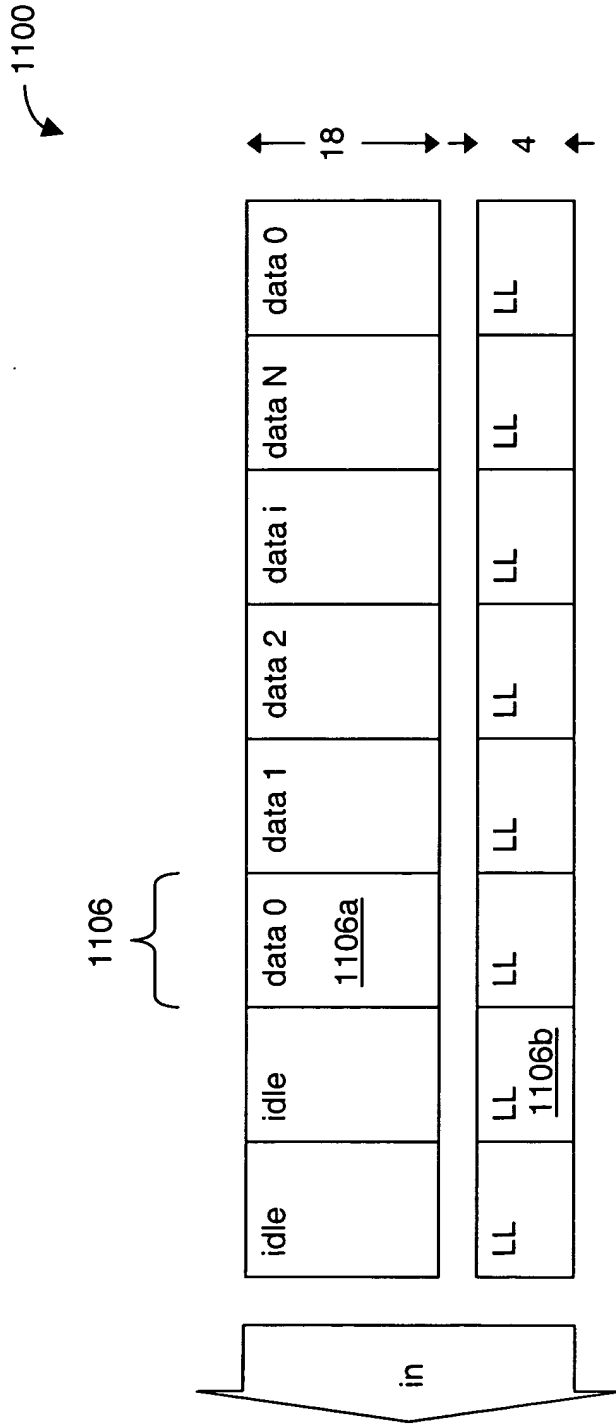


FIG. 11

↓Transfer	BITS 17:0
0	Lower Order Address Bits and Read/Write Command
1	Higher Order Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Stream ID,
3	Size Bits, Cancel Command, Priority, etc.

FIG. 13

↓Transfer	BITS 17:0
0	Lower Order Address Bits and Read/Write Command
1	Higher Order Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Size Bits, etc.
3	

FIG. 14

↓Transfer	BITS 17:0
0	Lower Order Configuration Address Bits and Read/Write Command
1	Higher Order Configuration Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, etc.
3	

FIG. 15

1600

LL signals	Transfers 0:3
0	Info and Check Bits
1	Header, Tail, and Check Bits
2	Extended Mode Bits
3	

FIG. 16

1700

LL signals	Transfers 0:3
0	Type and Check Bits
1	
2	Info and Check Bits
3	

FIG. 17

+

1800

LL signals	Transfers 0:3
0	Tag, Control, and Check Bits
1	
2	Tag, Info, and Check Bits
3	

FIG. 18

FIG. 19

1900

FIG. 19

2000

LL signal

FIG. 20

+